WHAT IS CLAIMED IS:

1. A magnetic recording/reproducing apparatus comprising a perpendicular magnetic recording double-layer medium with a soft magnetic underlayer and a reproducing head constituted by a magneto resistive effect type head with a shield film,

wherein a reproduced signal outputted from said reproducing head is processed through a partial response equalization circuit having a frequency characteristic so that a low-frequency component of said reproduced signal including a direct current component is passed and suppressed through said partial response equalization circuit; and

wherein said reproduced signal is supplied to a maximum-likelihood decoder so as to be data-reproduced.

2. A magnetic recording/reproducing apparatus according to Claim 1, wherein reproduced waveforms corresponding to a pair of the two closest recording transitions recorded on said recording medium at a shortest bit length interval are outputted as a waveform having intersymbol interference with amplitude ratios (A_1, A_2, A_3,…, A_k,…, A_N) (k is an integer indicating a bit interval, and A_1 and A_N are non-zero real numbers with opposite signs: $A_1+A_2+A_3\ldots+A_k+\ldots.+A_N \neq 0$, $N \geqq 2$) at each bit interval through said partial response equalization circuit, or as a dipulse waveform having asymmetrical amplitudes with opposite polarities

through said partial response equalization circuit; and wherein said outputted waveforms are supplied to said maximum-likelihood decoder so as to be data-reproduced.

3. A magnetic recording/reproducing apparatus according to Claim 2,

wherein said reproduced waveform corresponding to a pair of the closest two recording transitions recorded on said recording medium at a shortest bit length interval are outputted as a waveform having intersymbol interference with amplitude ratios (P_1, $P_2-\alpha P_1, \ldots$, $P_k-\alpha P_{k-1}, \ldots$, $P_N-\alpha P_{N-1}$, $-\alpha P_N$) (α is a value of a real number in a range of $0 \leq \alpha \leq 1$, <u>k</u> is an integer indicating a bit interval, $P_1, P_2, \ldots$, $P_k \ldots, P_N$ are real numbers with the same sign, and P_1 and P_N: non-zero real numbers: $N \geqq 2$) at each bit interval through said partial response equalization circuit; and

wherein said outputted waveforms are supplied to said maximum-likelihood decoder so as to be data-reproduced.

4. A magnetic recording/reproducing apparatus according to Claim 3, wherein said partial response equalization circuit comprises: an operation circuit which operates to subtract a signal value obtained in a manner so that each input signal supplied to said equalization circuit is delayed by a predetermined bit time and the delayed input signal is increased by α times, from said input signal; and a predetermined waveform processing circuit.

5. A magnetic recording/reproducing apparatus according to Claim 3, wherein a value of a parameter α not smaller than 0.1 is used.

6. A magnetic recording/reproducing apparatus according to Claim 1, comprising a plurality of partial response equalization circuits having different direct current frequency component passing characteristics respectively or a plurality of partial response equalization circuits defined by different values of parameter α respectively,

wherein a reproduced signal from said reproducing head is supplied to said plurality of partial response equalization circuits so as to be waveform-equalized in said partial response equalization circuits.

7. A magnetic recording/reproducing apparatus according to Claim 1, wherein one of different direct current frequency component passing characteristics or one of different values of parameter α is selected and set in said partial response equalization circuit, and wherein said reproduced signal from said reproducing head is supplied to said partial response equalization circuit so as to be waveform-equalized.

8. A magnetic recording/reproducing apparatus according to Claim 6, wherein at least one of said different direct current frequency component passing characteristics is a cut-off characteristic of a direct current frequency component, or at least one of

different values of said parameter α satisfies a condition of $\alpha=1$.

9. A magnetic recording/reproducing apparatus according to Claim 8, wherein a signal for adjusting or controlling a circuit disposed in a pre-stage of said partial response equalization circuit is referred to from a circuit in a post-stage of said partial response equalization circuit having said cut-off characteristic of said DC frequency component, or from a circuit in a post-stage of said response equalization circuit having said parameter α satisfying $\alpha=1$.

10. A magnetic recording/reproducing apparatus according to Claim 1, wherein an information data bit sequence to be recorded is converted into a data bit sequence so that a maximum number m of consecutive recording transitions recorded at a shortest bit length interval on said recording medium is limited to a finite value, and then said converted data bit sequence is recorded on said recording medium.

11. A magnetic recording/reproducing apparatus according to Claim 10, wherein said maximum number m of consecutive recording transitions is limited to be not larger than 4.

12. A magnetically recorded/reproduced signal processing circuit mounted on a perpendicular magnetic recording/reproducing apparatus using a perpendicular magnetic recording double-layer film medium with a soft magnetic underlayer and a reproducing head constituted

by a magneto resistive effect type head with a shield film,

wherein a reproduced signal outputted from said reproducing head is processed through a partial response equalization circuit having a frequency characteristic so that a low-frequency component of said reproduced signal including a direct current component is passed and suppressed through said partial response equalization circuit; and

wherein said reproduced signal outputted from said partial response equalization circuit is supplied to a maximum-likelihood decoder so as to be data-reproduced.

13. A magnetically recorded/reproduced signal processing circuit according to Claim 12,

wherein reproduced waveforms corresponding to a pair of the closest two recording transitions recorded on said recording medium at a shortest bit length interval are passed through said partial response equalization circuit so as to be outputted as a waveform having intersymbol interference with amplitude ratios (A_1, A_2, A_3,..., A_k,..., A_N) (**k** is an integer indicating a bit time interval, and A_1 and A_N are non-zero real numbers with opposite signs: $A_1+A_2+A_3...+A_k+....+A_N \neq 0$, $N \geqq 2$) at each bit interval through said partial response equalization circuit, or as a dipulse waveform having asymmetrical amplitudes with opposite polarities through said partial response

equalization circuit; and

wherein said outputted waveforms are supplied to said maximum-likelihood decoder so as to be data-reproduced.

14. A magnetically recorded/reproduced signal processing circuit according to Claim 13,

wherein said reproduced waveform corresponding to a pair of the closest two recording transitions recorded on said recording medium at a shortest bit length interval is passed through said partial response equalization circuit so as to be outputted as a waveform having intersymbol interference with amplitude ratios (P_1, $P_2-\alpha P_1, \ldots$, $P_k-\alpha P_{k-1}, \ldots$, $P_N-\alpha P_{N-1}$, $-\alpha P_N$) (α is a value of a real number in a range of $0 \leq \alpha \leq 1$, k is an integer indicating a bit time interval, $P_1, P_2, \ldots$, $P_k \ldots, P_N$ are real numbers with the same sign, and P_1 and P_N: non-zero real numbers: $N \geqq 2$) at each bit interval through said partial response equalization circuit; and

wherein said outputted waveforms are supplied to said maximum-likelihood decoder so as to be data-reproduced.

15. A magnetically recorded/reproduced signal processing circuit according to Claim 14, wherein said partial response equalization circuit comprises: an operation circuit which operates to subtract a signal value obtained in a manner so that each input signal supplied to said equalization circuit is delayed by a

predetermined bit time and the delayed input signal is increased by α times, from said input signal; and a predetermined waveform processing circuit.

16. A magnetically recorded/reproduced signal processing circuit according to Claim 12, wherein a value of a parameter α not smaller than 0.1 is used.

17. A magnetically recorded/reproduced signal processing circuit according to Claim 12 comprising a plurality of partial response equalization circuits having different direct current frequency component passing characteristics respectively or a plurality of partial response equalization circuits defined by different values of a parameter α respectively, wherein a reproduced signal from said reproducing head is supplied to said plurality of partial response equalization circuits so as to be waveform-equalized in said partial response equalization circuits.

18. A magnetically recorded/reproduced signal processing circuit according to Claim 12, wherein one of different direct current frequency component passing characteristics or one of different values of a parameter α is selected and set in said partial response equalization circuit, and wherein said reproduced signal from said reproducing head is supplied to said partial response equalization circuit so as to be waveform-equalized.

19. A magnetically recorded/reproduced signal processing circuit according to Claim 17, wherein at

least one of said different direct current frequency component passing characteristics is a cut-off characteristic of a direct current frequency component, or at least one of different values of said parameter α satisfies a condition of $\alpha=1$.

20. A magnetically recorded/reproduced signal processing circuit according to Claim 19, wherein a signal for adjusting or controlling a circuit disposed in a pre-stage of said partial response equalization circuit is referred to from a circuit in a post-stage of said partial response equalization circuit having said cut-off characteristic of said DC frequency component, or by a circuit in a post stage of said response equalization circuit having said parameter α satisfying $\alpha=1$.

21. A magnetically recorded/reproduced signal processing circuit according to Claim 12, further comprising a bit processing circuit or bit modulation circuit for performing a bit conversion process to an information data bit sequence recorded on said recording medium so that a maximum number m of consecutive recording transitions recorded at a shortest bit length interval on said medium is limited to a finite value; and another bit processing circuit or bit detection circuit for performing an inverse process to said bit conversion process to said recorded data bit sequence reproduced from said recording medium.

22. A magnetically recorded/reproduced signal processing circuit according to Claim 21, wherein said maximum number m of consecutive recording transitions is limited to be not larger than 4.

23. A semiconductor integrated circuit, wherein a magnetically recorded/reproduced signal processing circuit described in Claim 12 is mounted thereon.

24. A magnetic recording/reproducing apparatus, wherein a semiconductor integrated circuit stated in Claim 23 is mounted thereon.